AMENDMENTS TO THE CLAIMS

Claims 1-3 (canceled)

Claim 4 (currently amended) The invention of ~~Claim 3~~ Claims 9, wherein said resistive network further includes a first plurality of switches S_1, S_2, ...S_m, each switch coupled to one of said first plurality of resistors R_a, R_b, ..., R_m and adapted to switch said resistor in and out of said resistive network in response to said control signal.

Claim 5 (original) The invention of Claim 4 wherein said control signal is a digital word comprised of m bits.

Claim 6 (original) The invention of Claim 5 wherein each bit of said control signal controls one of said switches S_1, S_2, ...S_m.

Claim 7 (currently amended) The invention of ~~Claim 3~~ Claim 9, wherein said first plurality of resistors R_a, R_b, ..., R_m are binarily weighted.

Claim 8 (currently amended) The invention of ~~Claim 3~~ Claim 9, wherein said resistive network further includes a resistor R2 connected between node A and node B.

Claim 9 (currently amended) ~~The invention of Claim 3~~ A current source comprising:

first means for generating a current in response to an applied voltage and a resistance variable in response to a control signal; and

second means for supplying said control signal,

wherein said first means includes a resistive network comprising a first plurality of resistors R_a, R_b, ..., R_m,

wherein said first plurality of resistors R_a, R_b, ..., R_m are connected in parallel across a first node A and a second node B, and

wherein said resistive network further includes two resistors R_A and R_B connected in series between node A and node B.

Claim 10 (original) The invention of Claim 9 wherein said resistive network further includes a second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk}.

Claim 11 (original) The invention of Claim 10 wherein said second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk} are connected in parallel across resistor R_B.

Claim 12 (original) The invention of Claim 11 wherein said resistive network further includes a second plurality of switches S_{B1}, S_{B2}, ...S_{Bk}, each switch coupled to one of said second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk} and adapted to switch said resistor in and out of said resistive network in response to said control signal.

Claim 13 (currently amended) ~~The invention of Claim 3~~ A current source comprising:

first means for generating a current in response to an applied voltage and a resistance variable in response to a control signal; and

second means for supplying said control signal,

wherein said first means includes a resistive network comprising a first plurality of resistors R_a, R_b, ..., R_m,

wherein said first plurality of resistors R_a, R_b, ..., R_m are connected in parallel across a first node A and a second node B, and

wherein said resistive network further includes a third plurality of resistors R_A, R_B, ...R_L connected in series between node A and node B.

Claim 14 (original) The invention of Claim 13 wherein said resistive network further includes one or more resistor banks, each resistor bank including a number of resistors R_{B1}, R_{B2}, ..., R_{Bk}.

Claim 15 (original) The invention of Claim 14 wherein said resistor banks are each connected in parallel across one or more of said third plurality of resistors R_A, R_B, ...R_L.

Claim 16 (original) The invention of Claim 15 wherein said resistors R_{B1}, R_{B2}, ..., R_{Bk} of said resistor banks are connected in parallel.

Claim 17 (original) The invention of Claim 16 wherein each of said resistor banks further includes a number of switches S_{B1}, S_{B2}, ...S_{Bk}, each switch coupled to one of said resistors R_{B1}, R_{B2}, ..., R_{Bk} and adapted to switch said resistor in and out of said resistive network in response to said control signal.

Claim 18 (original) The invention of Claim 4 wherein said switches are implemented using transistors.

Claim 19 (original) The invention of Claim 18 wherein said switches are implemented using NMOS transistors.

Claim 20 (original) The invention of Claim 18 wherein the number of transistors used to implement each switch is determined by the weight of the resistor that the switch is coupled to.

Claim 21 (original) The invention of Claim 18 wherein said switches are controlled by control signals applied to the gates of said transistors.

Claim 22 (currently amended) The invention of ~~Claim 2~~ Claim 9 or 13 wherein said first means further includes a transistor Q adapted to apply a voltage across said resistive network to generate a current I.

Claim 23 (original) The invention of Claim 22 wherein a reference voltage V_{REF} is applied to the base of said transistor Q.

Claim 24 (original) The invention of Claim 22 wherein said current I is output from the collector of said transistor Q.

Claims 25-31 (canceled)

Claim 32 (currently amended) The invention of ~~Claim 31~~ Claims 36, 37, or 38 wherein said DAC is a voltage output DAC adapted to change the voltage at said node between R1 and R3.

Claim 33 (currently amended) The invention of ~~Claim 31~~ Claims 36, 37, or 38 wherein said DAC is a current output DAC adapted to add a current at said node between R1 and R3.

Claim 34 (canceled)

Claim 35 (currently amended) The invention of ~~Claim 31~~ Claims 36, 37, or 38 wherein a reference voltage V_{REF} is applied to the base of said transistor Q.

Claim 36 (currently amended) ~~The invention of Claim 34~~

A current source comprising:

two resistors R1 and R3 connected in series;

first means for applying a voltage across said resistors R1 and R3 to generate a current I, wherein said first means includes a transistor Q, and;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

second means for supplying said control signal,

wherein said current I is output from the collector of said transistor Q

Claim 37 (currently amended): ~~The invention of Claim 34~~ A current source comprising:

two resistors R1 and R3 connected in series;

first means for applying a voltage across said resistors R1 and R3 to generate a current I, wherein said first means includes a transistor Q, and;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

second means for supplying said control signal,

wherein said resistor R1 is coupled to the emitter of said transistor Q.

Claim 38 (currently amended): ~~The invention of Claim 34~~ A current source comprising:

two resistors R1 and R3 connected in series;

first means for applying a voltage across said resistors R1 and R3 to generate a current I, wherein said first means includes a transistor Q, and;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

second means for supplying said control signal,

wherein said resistor R3 is connected ground.

Claim 39 (original): A current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistor R1 connected to the emitter of transistor Q;

a resistor R3 having one end connected in series to R1 and the other end connected to ground;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

a circuit for supplying said control signal.

Claim 40 (original): A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current steering cells, each cell including:

a current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistor R1 connected to the emitter of transistor Q;

a resistor R3 having one end connected in series to R1 and the other end connected to ground;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

a circuit for supplying said control signal; and

a pair of transistors for selectively switching current from said current source between said first current summing bus and said second current summing bus in response to an input signal.

Claims 41-42 (canceled)